UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/662,832	09/15/00	VAN HOOK	T 1778.0100002

TM01/0824
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EXAMINER	
PAN, D	
ART UNIT	**PAPER NUMBER**
2183	8

DATE MAILED: 08/24/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/662,832	Van Hook et al.
Examiner	**Art Unit**
Pan	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *09/15/01,04/09/01*

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1 and 49-53* is/are pending in the applica

4a) Of the above, claim(s) *clams 2-48 have been canceled* is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1, 49, and 52* is/are rejected.

7) ☒ Claim(s) *50, 51, and 53* is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

Claims 1, 49-53 are presented for examination. Claims 2-48 have been canceled.

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claim 1, it is not clear what "the bits" in the second register (see claim 1, line 14) is referring to. Is it referring to the first byte of the second register, or is it referring to the first bit of the second byte ?

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claim 1 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,266,758. Although the conflicting claims are not identical, they are not patentably distinct from each other because while claim 1 of the current case present additional feature of "the first vector contains a first byte of an

aligned vector to be generated" than the patented claim 1, it would have been obvious to one of ordinary skill in the art to recognize the first vector was capable of containing the first byte of the aligned vector based on the determining step of determining a starting byte in the first register which specified the first byte of the aligned vector (see determining steps in both cases in claims 1), and because the general feature (patented claim) of determining the starting byte, which specified the first byte in the aligned vector, would be applicable to any specific vector, such as first or Nth vector, loaded into the first register (see the loading of first vector in first register in claim 1 lines 7 of current case).

3. Claim 1 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 5,933,650. Although the conflicting claims are not identical, they are not patentably distinct from each other because while the current claim 1 presents the additional feature of "the starting byte is specified as a constant in alignment instruction" than the patented claim 1, it would have been obvious to one of ordinary skill in the art to specify the starting byte as a constant because the determination step of current claim 1 generally encompassed any type of starting byte, such as variable or constant and one of ordinary skill in the art should be able to use either a varable or a constant in the firast byte based on these two only choices available in the art at the tiem the claimed invention was made. .

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,49,52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. (5,887,183) in view of Cho et al. (5,922,066).

As to claim 1, Agarwal disclosed a system (fig.4A) comprising at least :

a)loading a first vector [X] from a memory into a vector register [Vri](see fig.4A; see col.13, lines 13-50, see also fig.6A, col.11, lines 46-50 for real and imaginary elements in respective registers, and the loading of even and odd number vector elements in col.13, lines 10-25);

b)loading a second vector [X+1] into a second register (see the subsequent vector loading in fig.4A; see col.13, lines 13-50);

c)determining a starting byte [32 bits] in a fist register wherein the starting byte specifies the first byte [32] of an aligned vector [64 bit](e.g. see the use of byte or word col.15, lines 15-30, see also the aligned vector in col.15, lines 31-67, col.16, lines 1-14);

d)extracting a first width vector [64 bit] from a first register beginning from the first bit [higher/lower bit] continuing through a bit in second register (e.g. see the consecutive single precision elements in col.15, lines 44-50).

Agarwal did not specifically show the replication of the first width vector into a third register as claimed. However, Cho disclosed a system including replicating a first width vector [vector operand] into a third register [resultant vector register] (e.g. see the shifting into the resultant vector in col.5, lines 14-20). It would have been obvious to one of ordinary skill in the art to use Cho in Agarwal for replicating the extracted vector into the third register as claimed because the use of Cho could provide predetermined vector format, such as aligned vector, for a given operation, such as read/write, at particular word length in the execution of the instruction sequence, and it could be readily done by selecting partial vectors, such as word , or byte, of the data elements into a newly aligned vector register in Agarwal.

As to claim 49, Agarwal disclosed at least :

a) a)loading a first vector [X] from a memory into a vector register [Vri](see fig.4A; see col.13, lines 13-50 , see also fig.6A, col.11, lines 46-50 for real and imaginary elements in respective registers and the loading of even and odd number vector elements in col.13, lines 10-25);

b)loading a second vector [X+1] into a second register (see the subsequent vector loading in fig.4A; see col.13, lines 13-50);

c)reading a first plurality of elements [VRi] from a first register [260] and second plurality of elements [Vri+1] from a second register[262] (see col.11, lines 56-67, col.12, lines 1-10).

Agarwal did not specifically show the writing of the first plurality of elements and second plurality of elements into a third register in particular order as claimed. However, Cho disclosed a

system including writing a first plurality of elements [vector operand A] and second plurality of elements [vector operand B] into a third register [resultant vector register] (e.g. see the shifting into the resultant vector in col.5, lines 14-20). It would have been obvious to one of ordinary skill in the art to use Cho in Agarwal for writing the first and second into the third register as claimed because the use of Cho could enhance the control of a predetermined vector format, such as aligned vector, for a given processing, such as read/write, at specific word width in the operation of the execution of the instruction sequence, and it could be readily achieved by selecting partial vector elements, such as word , or byte, of the data vector into a newly aligned vector register in Agarwal.

As to claim 52, Agarwal disclosed at least :

a)loading a first source vector [X] from a memory into a vector register [Vri](see fig.4A; see col.13, lines 13-50 , see also fig.6A, col.11, lines 46-50 for real and imaginary elements in respective registers and the loading of even and odd number vector elements in col.13, lines 10-25);

b)loading a second source vector [X+1] into a second register (see the subsequent vector loading in fig.4A; see col.13, lines 13-50,see also fig.6A, col.11, lines 46-50 for real and imaginary elements in respective registers and the loading of even and odd number vector elements in col.13, lines 10-25).

Agarwal did not specifically show the selection of the first subset of element and the selection of the second subset of elements comprising the combination of odd, even, lower or upper as claimed. Instead Agarwal disclosed only a combination of even and odd subset of data elements (see col.13, lines 10-25). However, Cho disclosed an input selection circuit [310] for selecting a first and a second data elements (see col.5, lines 11-20). It would have been obvious to one of ordinary skill in the art to use Cho in Agarwal for selecting the first and second plurality of elements as claimed because the use of Cho could increase the flexibility of loading the vector elements to accept to different order of the input vector, such as even or odd data elements, at a specific sequence of the input vectors, and it could be done by inserting a selector into the vector register interface unit of Agarwal to adaptively select the either the first or second vectors from the vector registers.

Claims 50,51,53 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel Pan, Esq. whose telephone number is (703) 305 9696. The examiner can normally be reached on M-F from 8:00 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Chan, can be reached on (703) 305 9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 305 3718.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305 3900.

DANIEL H PAN
PRIMARY EXAMINER
GROUP